REMARKS

Reconsideration of this application, as amended, is respectfully requested. The following remarks are responsive to the Office Action mailed June 20, 2006.

35 USC §102 Rejections

Claims 1, 2, 4-8, 10-15, 17, and 18 are rejected under 35 U.S.C. §102(b) as being anticipated by Hirata et al., U.S. Patent Number 5,430,851. Specifically, the Office Action asserts that Hirata teaches a scheduler having at least two stages, the first of which to, *inter alia*, map instruction groups to particular functional groups and the second of which to, *inter alia*, merge the instruction groups and remap them to particular functional groups. In support of this assertion, the Office Action cites feature 14 (Instruction Setup Unit of Hirata) of Figure 3, which the Office Action claims to embody the function claimed in claim 1 regarding the first stage, and feature 15 (Instruction Scheduling Unit of Hirata), which the Office Action claims to embody the function claimed in claim 1 regarding the second stage.

Applicant, however, submits that Hirata does not teach performing mapping of instruction groups to functional units by one stage and merging/remapping of instruction groups to functional units by another stage, as claimed by Applicant. Particularly, contrary to the assertion in the Office Action, Hirata's Instruction Setup Unit does not perform any sort of instruction mapping to functional units, but instead only performs dependency analysis, decoding, and instruction fetching (see Figure 3). Any mapping of instructions to particular functional units is soley performed by a one-stage instruction schedule unit. This is precisely the type of scheduler described by Applicant in the

"Background" section of Applicant's disclosure (i.e., a scheduler that contains a high amount of dispersal logic so that instructions may be mapped in one stage).

Applicant claims in claim 1 and other independent claims that the mapping is to be performed using at least two stages, one for mapping the instructions to particular functional units and another to merge and remap the instructions to particular functional units. This, the Applicant explains in his disclosure, reduces the amount of dispersal logic necessary to map instructions to particular functional units possessed by prior art techniques, such as those embodied in Hirata. Therefore, Applicant submits that independent claims 1, 7, and 13 are not anticipated by Hirata.

It is respectfully asserted by Applicant that all presently standing claims are now in condition for allowance. Please charge any fees not covered by any checks submitted herewith to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Michael J. Mallie
36,591

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1030
(408) 720-8300